What is Claimed Is:

1. A method for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol, the method comprising:

receiving by an external logic unit an expansion port frame from the expansion port via an expansion bus;

generating by the external logic unit a new expansion port frame based on reception of the expansion port frame; and

outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip.

2. The method of claim 1, wherein the generating step includes changing data within the received expansion port frame to generate the new expansion port frame.

3. The method of claim 2, wherein the changing step includes:

parsing a header of the expansion port frame to retrieve a source address value from a source address field and a destination address value from a destination address field;

inserting the source address value into the destination address field, and the destination address value into the source address field, of the new expansion port frame.

4. The method of claim 3, wherein the changing step further includes inserting a new device identifier value, different from a value of an existing device identifier value in the received expansion port frame, into a device identifier field in the new expansion port frame.

5. The method of claim 4, wherein the external logic unit is implemented using a field programmable gate array.

6. The method of claim 1, wherein the external logic unit is implemented using a field programmable gate array.

7. A test system for testing a network switch chip having an expansion port configured for transferring data according to a prescribed protocol, the system comprising:

an expansion port bus configured for propagation of the expansion port frame output by the expansion port; and

an external logic unit configured for generating a new expansion port frame based on reception of the expansion port frame, and outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip.

8. The system of claim 7, wherein the external logic unit is configured for generating the new expansion port frame by changing data within the received expansion port frame.

9. The system of claim 8, wherein the external logic unit is configured for changing data by parsing a header of the expansion port frame to retrieve a source address value from a source address field and a destination address value from a destination address field, the external logic unit inserting the source address value into the destination address field, and the destination address value into the source address field, of the new expansion port frame.

10. The system of claim 9, wherein the external logic unit is configured for inserting a new device identifier value into a device identifier field in the new expansion port frame.

11. The system of claim 7, wherein the external logic unit is implemented using a field programmable gate array.